AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claim 13 without prejudice and amend claims 1-3, 5, 10-11 and 15-20 as follows:

LISTING OF CLAIMS:

1. (Currently Amended) A data processing system comprising:

a data transferring apparatus having data input and data output~~; a plurality of data transferring sections operable in parallel~~ for transferring data as data words having bit width which is a multiple M of the bit width of the input data~~, and a circuit for synchronising said parallel data transferring sections~~; and

a programmable frequency clock generator for generating a clock signal, wherein said programmed frequency includes a full-frequency and a low-frequency, the low frequency being a quotient 1/M of the full frequency ~~and the number of said data transferring sections~~;

wherein said data transferring ~~sections operate~~ apparatus operates at said low frequency; while said input and output data are provided at said full frequency.

2. (Currently Amended) The data processing system according to claim 1, wherein said data transferring ~~sections are~~ apparatus is a data ~~transmitters~~ transmitter.

3. (Currently Amended) The data processing system according to claim 1, further comprising a multiplexer for receiving data from said data transferring

~~sections~~ apparatus at said low frequency and providing output data at said full frequency.

4. (Original) The data processing system according to claim 1, when used as a test system, wherein said data is transferred at said full frequency for accessing a memory device under test.

5. (Currently Amended) The data processing system according to claim 1, wherein said data transferring ~~sections are~~ apparatus is a data ~~receivers~~ receiver.

6. (Original) The data processing system according to claim 1, wherein the data transferring apparatus comprises a plurality of data transmitting sections and a plurality of data receiving sections, wherein said data transmitting sections and said data receiving sections are operable at said low frequency; while said output and input data is transferred at said full frequency.

7. (Original) The data processing system as claimed in claim 1, wherein said low frequency is equal to a half of said full frequency.

8. (Original) The data processing system as claimed in claim 1, wherein said low frequency is equal to one forth of the full frequency.

9. (Original) The data processing system as claimed in claim 1, further comprising a resynchronisation circuit for resynchronising data received at low frequency to a system clock signal of full frequency.

10. (Currently Amended) A method of data processing comprising the steps of:

providing input data and output data;

transferring data ~~through a plurality of parallel data transferring channels, wherein the data transfer additionally comprises synchronising said parallel data transferring channels~~ as data words having a bit width which is a multiple M of the bit widths of the input data;

generating clock signals of programmable frequency, wherein said programmed frequency includes full-frequency and low-frequency, the low frequency being a quotient 1/M of the full frequency ~~and the number of said data transferring channels~~,

wherein said operations of data transfer are performed at said low frequency, while said input and output data are provided at said full frequency.

11. (Currently Amended) The method of data processing according to claim 10, wherein ~~the data transferring sections are data transmitters,~~ the method further ~~comprising~~ comprises multiplexing data received ~~from said data transmitters~~ at said low frequency and providing multiplexed output data at said full frequency.

12. (Original) The method of data processing according to claim 10, wherein the data at said full frequency are provided for accessing memory device under test.

13. (Canceled)

14. (Original) The method of data processing according to claim 10, comprising the steps of transmitting data, latching transmitted data and supplying latched data to a plurality of receiving logic devices; wherein said operations of data transmission, latching data and receiving data are performed at said low frequency; while said input and output data are provided at said full frequency.

15. (Currently Amended) The method of data processing according to claim [[1]] 10, wherein said low frequency is equal to a half of said full frequency, for SDRAM memories.

16. (Currently Amended) The method of data processing according to claim [[1]] 10, wherein said low frequency is equal to one [[forth]] fourth of the full frequency, for DDR memories.

17. (Currently Amended) The method of data processing according to claim [[1]] 10, further comprising a step of resynchronisation of data received at low frequency to a system clock signal of full frequency.

18. (Currently Amended) A test system comprising:

an algorithmic pattern generator ~~having a plurality of test data generating sections operable in parallel for~~ generating test data as data words having a bit width which is a multiple M of the bit width required for accessing a memory device under test~~, wherein the pattern generator additionally comprises a circuit for synchronising said parallel data generating sections~~;

a programmable frequency clock generator for generating a clock signal, wherein said programmed frequency includes a full-frequency and a low-frequency, the low frequency being a quotient 1/M of the full frequency ~~and a number of said test data generating sections~~;

a multiplexer that receives ~~said~~ a wide test data word ~~from said data generating sections~~ at said low frequency and ~~provides multiplexed~~ multiplexes said wide data word into multiple frequency to access ~~for accessing~~ DUT at said full frequency;

a plurality of registers for latching data from the DUT and supplying latched fault data to a plurality of fault logic devices;

wherein said ~~test data generating sections, said registers~~ algorithmic pattern generator and said fault logic devices operate at said low frequency; while said registers access the device under test ~~is accessed~~ at said full frequency.

19. (Currently Amended) The test system as claimed in claim 18, wherein said low frequency is equal to a half of said full frequency~~, for example,~~ for SDRAM memories.

20. (Currently Amended) The test system as claimed in claim 18, wherein said low frequency is equal to one [[forth[[fourth of the full frequency, for DDR memories.